UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,904	09/28/2001	J. G. Walacavage	200-0665	4251

7590 02/14/2007

Daniel H. Bliss
Bliss McGlynn P.C.
2075 West Big Beaver Road Suite 600
Troy, MI 48084

EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/965,904	WALACAVAGE ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/2/06,10/19/06,1/26/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-15 were rejected in the office action of 25 August 2006. In response, Applicants have amended claims 9 and 15. Claims 1-15 are pending in this application.

Claims 1-15 are rejected.

Information Disclosure Statement

The Information Disclosure Statement filed on 19 October 2006 references this application serial number, 09/965,904, on the cover sheets. The attached form PTO-1449 references a different application serial number, 09/965,905. The references on cited on this form PTO-1449 have been lined through. These references have been previously cited on the Information Disclosure Statement filed on 2 October 2006, which has been considered by the Examiner.

The 19 October 2006 Information Disclosure Statement may have been submitted for this application in error.

Response to Arguments – 35 USC § 103

1. In response to the previous rejections of claims 1-15 under 35 U.S.C. § 103 as being unpatentable over Banks in view of Schruben, Applicants argue primarily that:

> Banks does not disclose constructing a flowchart that describes interaction of an operator in a workcell using a computer wherein such interaction comprises sequential operations and asynchronous operations and modeling the operator as an input to a programmable logic controller (PLC) by writing a control model of the operator interaction in the workcell based on predefined conditions described in the flowchart. (emphasis in original)

The Examiner respectfully traverses this argument as follows.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The previous rejection clearly set forth which teachings are found in the Banks reference and which teachings are found in the Schubert reference. The limitations referred to by Applicants' argument are rejected based on a combination of the references, not merely the Banks reference.

2. Applicants further argue that:

> Banks also does not disclose testing the control model by a PLC logical verification system on the computer as to whether PLC logic for the workcell is correct. (emphasis in original)

The Examiner respectfully traverses this argument as follows.

The previous rejection explicitly set forth that:

Banks teaches testing as to whether PLC logic for the workcell is correct [*"In either case the control system contains decision-making logic that should be tested as early as possible in the design of the system... The earlier that control system defects can be found, the better the material handling system will operate."* (page 539, Section 14.3.6 Control Systems)]. In the context of the Banks reference, it would be clear to a person of ordinary skill in the art that the control system is a computer system. A system that verifies PLC logic is a "PLC logical verification system." The claim does not specify and Applicants have not explicitly and deliberately defined a special meaning for this term.

3. Applicants further argue that:

> Banks further does not disclose loading the PLC logic in the PLC controlling the workcell if the PLC logic for the workcell is correct and using the PLC logic by the PLC to operate the workcell. (emphasis in original)

The Examiner respectfully traverses this argument as follows.

The previous rejection explicitly set forth that:

Banks teaches loading the PLC logic in the PLC controlling the workcell if the PLC logic for the workcell is correct and using the PLC logic by the PLC to operate the workcell [*"Some simulation tools can actually communicate with control system programs directly to help test the code."* (page 539, Section 14.3.6 Control Systems)]. In the context of the Banks reference, it would be clear to a person of ordinary skill in the art that the purpose of simulation and direct interaction with control system programs is for the purpose of loading the PLC logic in the PLC controlling the workcell. This end result is the motivation for the entire process described by Banks, as would be apparent to a person of ordinary skill in the art.

4. Applicants further argue that:

> Schruben does not disclose constructing a flowchart that describes interaction of an operator in a workcell using a computer wherein such interaction comprises sequential operations and asynchronous operations. (emphasis in original)

The Examiner respectfully traverses this argument as follows.

The previous rejection explicitly set forth that:

Schruben discloses constructing a flowchart that describes interaction of an operator in a workcell wherein such interaction comprises sequential operations and asynchronous operations [*"System Description: An operator is responsible for loading and unloading parts that are processed by a machine as well as freeing a jammed machine."* Sequential operations: *"The machine is loaded and unloaded requiring times t_l and t_u, respectively. The time required for the*

machine to cycle is t_c." Asynchronous operations: *"The (random) machine run-time until the next time the machine jams is denoted by t_j. The (random) time required to repair a jammed machine is denoted by t_r."* (all from page 959, left column, first paragraph); Flowchart: *"FIGURE 2. Event graph for the Semiautomatic Machine System. Event vertices and state variables are defined in the text."* (page 959, right column, lower right corner)]. In the context of the Banks and Schruben references, it would be clear to a person of ordinary skill in the art that the described methods are to be implemented on computer systems. The Examiner does not understand the novelty of Applicants' invention to lie in merely implementing a previously manual activity on a computer system.

5. Applicants further argue that:

> Schruben also does not disclose modeling the operator as an input to a programmable logic controller (PLC) by writing a control model of the operator interaction in the workcell based on predefined conditions described in the flowchart. (emphasis in original)

The Examiner respectfully traverses this argument as follows.

The previous rejection explicitly set forth that:

Schruben discloses modeling the operator as an input to a machine by writing a control model of the operator interaction in the workcell based on predefined conditions described in the flowchart [*"An operator is responsible for loading an unloading parts that are processed by a machine as well as freeing a jammed machine."* (page 959, left column); *"State variable definition, event definition, and edge conditioning usually proceed simultaneously in developing an event graph."* (page 960, left column, second paragraph); *"An event graph may be used to guide the development of an event-scheduling simulation program. For simple simulation models like the ones considered here, program development may proceed by visually checking*

the event graph to insure that the simulation model is logically "tied together." For more complex models, a system analysis of the event graph may be helpful." (page 960, left column, third paragraph); Sections 3-3.4].

6. Applicants further argue that:

> Banks lacks constructing a flowchart that describes interaction of an operator in a workcell using a computer wherein such interaction comprises sequential operations and asynchronous operations and modeling the operator as an input to a programmable logic controller (PLC) by writing a control model of the operator interaction in the workcell based on predefined conditions described in the flowchart. (emphasis in original)

The Examiner respectfully submits that this argument has been traversed above.

7. Applicants further argue that:

> Banks also lacks testing the control model by a PLC logical verification system on the computer as to whether the PLC logic for the workcell is correct and loading the PLC logic in the PLC controlling the workcell if the PLC logic for the workcell is correct. (emphasis in original)

The Examiner respectfully submits that this argument has been traversed above.

8. Applicants further argue that:

> In Banks, there is no logical modeling of operator interaction with a programmable logic controller logical verification system and there are no asynchronous operations of the operator. Also in Banks, there is no modeling of an operator as an input to a programmable logic controller (PLC). Further, Banks is not used to debug PLC logic. (emphasis in original)

The Examiner respectfully traverses this argument as follows.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The previous rejection clearly set

forth which teachings are found in the Banks reference and which teachings are found in the Schubert reference. The limitations referred to by Applicants' argument are rejected based on a combination of the references, not merely the Banks reference.

Further, the claim language does not recite "debugging PLC logic".

9. Applicants further argue that:

> Schruben merely discloses that an event graph can be used to develop alternative event-oriented representations of a system in which several candidate model structures can be considered for possible implementation as discrete-event simulations using an event-scheduling approach. Schruben lacks constructing a flowchart that describes interaction of an operator in a workcell using a computer wherein such interaction comprises sequential operations and asynchronous operations. (emphasis in original)

The Examiner respectfully traverses this argument as follows.

The previous rejection explicitly set forth that:

Schruben discloses constructing a flowchart that describes interaction of an operator in a workcell wherein such interaction comprises sequential operations and asynchronous operations [*"System Description: An operator is responsible for loading and unloading parts that are processed by a machine as well as freeing a jammed machine."* Sequential operations: *"The machine is loaded and unloaded requiring times t_l and t_u, respectively. The time required for the machine to cycle is t_c."* Asynchronous operations: *"The (random) machine run-time until the next time the machine jams is denoted by t_j. The (random) time required to repair a jammed machine is denoted by t_r."* (all from page 959, left column, first paragraph); Flowchart: *"FIGURE 2. Event graph for the Semiautomatic Machine System. Event vertices and state variables are defined in the text."* (page 959, right column, lower right corner)].

10. Applicants further argue that:

> In Schruben, there is discrete event simulations, which are time based, and cannot account for asynchronous operations. Further, there is no modeling of an operator as an input to a programmable logic controller (PLC). As such, there is no suggestion or motivation in the art to combine Banks and Schruben together. (emphasis in original)

The Examiner respectfully traverses this argument as follows.

Applicants' conclusion that "discrete event simulations ... cannot account for asynchronous operations" does not find factual basis in the references or in what would be known to a person of ordinary skill in the art.

Further, the previous rejection explicitly set forth that:

Schruben discloses modeling the operator as an input to a machine by writing a control model of the operator interaction in the workcell based on predefined conditions described in the flowchart [*"An operator is responsible for loading an unloading parts that are processed by a machine as well as freeing a jammed machine."* (page 959, left column); *"State variable definition, event definition, and edge conditioning usually proceed simultaneously in developing an event graph."* (page 960, left column, second paragraph); *"An event graph may be used to guide the development of an event-scheduling simulation program. For simple simulation models like the ones considered here, program development may proceed by visually checking the event graph to insure that the simulation model is logically "tied together." For more complex models, a system analysis of the event graph may be helpful."* (page 960, left column, third paragraph); Sections 3-3.4].

11. Applicants further argue that:

> Further, neither reference allows for modeling of an operator as an input to a programmable logic controller (PLC). As such, there is absolutely no teaching of a level of skill in the programmable logic controller art that a method of logical modeling operator interaction with a programmable logic controller logical verification system includes the steps of constructing a flowchart that describes interaction of an operator in a workcell using a computer wherein such interaction comprises sequential operations and asynchronous

> operations, modeling the operator as an input to a programmable logic controller (PLC) by writing a control model of the operator interaction in the workcell based on predefined conditions described in the flowchart, and testing the control model of a PLC logical verification system on the computer as to whether PLC logic for the workcell is correct. (emphasis in original)

The Examiner respectfully submits that this argument has been addressed above.

12. Applicants further argue that:

> The Examiner may not, because he doubts that the invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in the factual basis. See In re Warner, 379 F. 2d 1011, 154 U.S.P.Q 173 (CCPA 1967).

The Examiner respectfully traverses this argument as follows.

The ground of rejection is based strictly upon the express teachings of the prior art and what those references fairly teach to one of ordinary skill in the art at the time of Applicants' invention.

13. Applicants further argue that:

> Unlike the prior art, the focus of the present invention is on the logical representation of the operator and not the visual or spatial representations of the operator.

The Examiner respectfully submits that the claim language of the independent claims does not reflect "the logical representation of the operator [in contrast to] the visual or spatial representations of the operator." As pertains to the operator, the independent claim 1 merely recites "constructing a flowchart that describes interaction of an operator in a workcell using a computer wherein such interaction comprises sequential operations and asynchronous operations" and "modeling the operator as an input to a programmable logic controller (PLC) by writing a control model of the operator interaction in the workcell based on predefined conditions described in the flowchart." The claim language makes no distinction whatsoever

between the claimed invention and "visual or spatial representations of the operator [as found in the prior art]."

14. Applicants further argue that:

> The Examiner has failed to show how the prior art suggested the desirability of modification to achieve Applicants' invention. Thus, the Examiner has failed to establish a case of prima facie obviousness. Therefore, it is respectfully submitted that claims 1 through 15 are allowable over the rejection under 35 U.S.C. § 103. (emphasis in original)

The Examiner respectfully traverses this argument as follows.

The previous rejection explicitly set forth that:

The motivation for [combining the references] would be to more accurately model a real system of interaction between an operator and a PLC-controlled machine [*"In discrete-event digital simulation modeling, an analogy is created between a system and a computer program."* (Schruben, page 957, first paragraph); *"The next example is an extension of the first one. A service interruption is modeled here without the use of event canceling edges... We consider a single semiautomatic machine (so the event attribute of machine number can be dropped) that is subject to random jamming."* (Schruben, page 958, right column, Section 2.2)] and to make simulations easier to develop [*"Event graphs should make event-scheduling simulations easier to develop."* (Schruben, page 963, Section 5)].

Applicants' arguments have been fully considered but have been found unpersuasive.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. Claims 1-15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over "Handbook of Simulation," edited by Jerry Banks (Banks) in view of "Simulation Modeling with Event Graphs" by Lee Schruben (Schruben).

Banks discloses a programmable logic controller verification system [*"Control systems are implemented in software that runs material handling systems. The control system can be as large and complex as a warehouse management system (WMS) or as simple as the programmable logic controller (PLC) that controls a set of conveyor sections. In either case the control system contains decision-making logic that should be tested as early as possible in the design of the system. Many simulation tools include languages that can be used to replicate control system algorithms. Some simulation tools can actually communicate with control system programs directly to help test the code. The earlier that control system defects can be found, the better the material handling system will operate."* (page 539, Section 14.3.6 Control Systems; entire Chapter 14)], comprising:

Writing a control model of the simulation entities [*"Many simulation tools include languages that can be used to replicate control system algorithms."* (page 539, Section 14.3.6 Control Systems)];

Testing as to whether PLC logic for the workcell is correct [*"In either case the control system contains decision-making logic that should be tested as early as possible in the design of the system... The earlier that control system defects can be found, the better the material handling system will operate."* (page 539, Section 14.3.6 Control Systems)]; and

Loading the PLC logic in the PLC controlling the workcell if the PLC logic for the workcell is correct and using the PLC logic by the PLC to operate the workcell [*"Some simulation tools can actually communicate with control system programs directly to help test the code."* (page 539, Section 14.3.6 Control Systems)].

Banks does not expressly teach constructing a flowchart that describes interaction of an operator in a workcell using a computer wherein such interaction comprises sequential operations and asynchronous operations; and

Modeling the operator as an input to a programmable logic controller (PLC) by writing a control model of the operator interaction in the workcell based on predefined conditions described in the flowchart.

Schruben discloses constructing a flowchart that describes interaction of an operator in a workcell wherein such interaction comprises sequential operations and asynchronous operations [*"System Description: An operator is responsible for loading and unloading parts that are processed by a machine as well as freeing a jammed machine."* Sequential operations: *"The machine is loaded and unloaded requiring times t_l and t_u, respectively. The time required for the machine to cycle is t_c."* Asynchronous operations: *"The (random) machine run-time until the next time the machine jams is denoted by t_j. The (random) time required to repair a jammed machine is denoted by t_r."* (all from page 959, left column, first paragraph); Flowchart: *"FIGURE 2. Event graph for the Semiautomatic Machine System. Event vertices and state variables are defined in the text."* (page 959, right column, lower right corner)];

Schruben discloses modeling the operator as an input to a machine by writing a control model of the operator interaction in the workcell based on predefined conditions described in the flowchart [*"An operator is responsible for loading an unloading parts that are processed by a machine as well as freeing a jammed machine."* (page 959, left column); *"State variable*

definition, event definition, and edge conditioning usually proceed simultaneously in developing an event graph." (page 960, left column, second paragraph); *"An event graph may be used to guide the development of an event-scheduling simulation program. For simple simulation models like the ones considered here, program development may proceed by visually checking the event graph to insure that the simulation model is logically "tied together." For more complex models, a system analysis of the event graph may be helpful."* (page 960, left column, third paragraph); Sections 3-3.4].

Schruben and Banks are analogous art because both are directed to the field of simulation of manufacturing systems.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to include the operator and operator's interaction with the PLC-controlled machinery in the PLC logical verification system taught by Banks. This modification could comprise a "simulated operator" pushing a START or RESTART button on a PLC-controlled machine after "freeing a jammed machine".

The motivation for doing so is would be to more accurately model a real system of interaction between an operator and a PLC-controlled machine [*"In discrete-event digital simulation modeling, an analogy is created between a system and a computer program."* (Schruben, page 957, first paragraph); *"The next example is an extension of the first one. A service interruption is modeled here without the use of event canceling edges... We consider a single semiautomatic machine (so the event attribute of machine number can be dropped) that is subject to random jamming."* (Schruben, page 958, right column, Section 2.2)] and to make

simulations easier to develop [*"Event graphs should make event-scheduling simulations easier to develop."* (Schruben, page 963, Section 5)].

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the Schruben and Banks references to obtain the claimed invention.

Regarding claim 2, Schruben teaches that the step of testing comprises starting a timer and determining whether the operator interaction of the flowchart is completed within a predetermined time [*"The (random) time required to repair a jammed machine is dentoed by t_r."* (page 959, left column)].

Regarding claim 3, Schruben teaches that the step of testing includes initializing the operator interaction of the flowchart prior to starting the timer [FIGURE 2, node 1, corresponding to Event 1 (page 959, right column)].

Regarding claim 4, Schruben teaches that the step of testing includes idling the operator prior to starting the timer [*"Parts arrive to be processed at (random) intervals of time of length t_a."* (page 959, left column); *"Event 1: (part arrival): $P = P + 1$, generate t_a."* (page 959, right column); The graph "idles" in the initial node until an event occurs].

Regarding claim 5, Banks teaches that the step of constructing comprises constructing a series of commands for the operator using the computer [*"Many simulation tools include*

languages that can be used to replicate control system algorithms." (page 539, Section 14.3.6 Control Systems); entire Chapter 14].

Regarding claim 6, Schruben teaches that the operator has at least one resource [*"Every hour the operator is entitled to a five-minute break, but will take the time only after completing any partially finished work and unloading the machine."* (page 959, left column)].

Regarding claim 7, Schruben teaches that the resource has at least one capability [*"An operator is responsible for loading and unloading parts that are processed by a machine as well as freeing a jammed machine."* (page 959, left column)].

Regarding claim 8, Schruben teaches that the step of testing includes executing the commands when a timer is started [*"Parts arrive to be processed at (random) intervals of time of length* t_a*."* (page 959, left column); FIGURE 2; The graph and simulation are defined in terms of timed intervals during which the operator's instructions are executed.].

Claims 9 and 10 recite a combination of limitations found in claims 1 and 2. As claims 1 and 2 are obvious over Banks in view of Schruben, claims 9 and 10 are similarly obvious.

Claims 11 and 12 recite limitations corresponding to claims 3 and 4. As claims 3 and 4 are obvious over Banks in view of Schruben, claims 11 and 12 are similarly obvious.

Claims 13 and 14 recite a combination of limitations found in claims 5-7. As claims 5-7 are obvious over Banks in view of Schruben, claims 13 and 14 are similarly obvious.

Claim 15 recites a combination of limitations found in claims 9-14. As claims 9-14 are obvious over Banks in view of Schruben, claim 15 is similarly obvious.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

jsp

2/4/07

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100